E-FUSE AND ANTI-E-FUSE DEVICE STRUCTURES AND METHODS

Abstract of the Disclosure

Standard photolithography is used to pattern and fabricate a final polysilicon wafer imaged structure which is smaller than normal allowable photo-lithographic minimum dimensions. Three different methods are provided to produce such sub-minimum dimension structures, a first method uses a photolithographic mask with a sub-minimum space between minimum size pattern features of the mask, a second method uses a photolithographic mask with a sub-minimum widthwise jog or offset between minimum size pattern features of the mask, and a third method is a combination of the first and second methods. Each of the three methods can be used with three different embodiments, a first embodiment is a polysilicon E-Fuse with a sub-minimum width polysilicon fuse line, a second embodiment is a work function altered/programmed self-aligned MOSFET E-Fuse with a sub-minimum width fuse line, and a third embodiment is a polysilicon MOSFET E-Fuse with a sub-minimum width fuse line which is programmed with a low trigger voltage snapback.

Figures

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